ABSTRACT OF THE DISCLOSURE

SWITCHED-CAPACITOR SAMPLE/HOLD HAVING REDUCED AMPLIFIER SLEW-RATE AND SETTLING TIME REQUIREMENTS

A switched-capacitor sample/hold circuit and method having reduced slew-rate and settling time requirements provides for lower-cost and/or lower-power implementation of sample/hold circuits and/or reduced error due to amplifier characteristics. The switched-capacitor sample/hold circuit incorporates a pair of capacitors that are alternatively and mutually-exclusively switched between an input sample position and an amplifier hold position, providing a dual sampled amplifier output signal that has reduced transitions at each sample interval. An alternative embodiment of the sample/hold circuit incorporates a fully-differential amplifier having a differential input and a differential output. Four capacitors are employed forming two of the dual sampled switched-capacitor circuits, one in each negative feedback path (inverted output to non-inverting input, non-inverted output to inverting input) of the amplifier. The two dual sampled switched-capacitor circuits are referenced to each other, providing fully differential operation and cancellation of error due to charge injection.